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Please replace the paragraph on page 6, lines 7-9, with the following revised paragraph:

B¹

--FIGS. 3a through 3d, schematically illustrate a series of cross-sectional representations which illustrate the progressive stages in completing the fabrication of a FET device in accordance with a process of the present invention.--

Please replace the paragraph on page 8, starting at line 4 with the following revised paragraph:

B²

--Generally, although not necessary for the practice of the invention, further materials may be deposited to form additional material layers upon the polysilicon layer 18 of the gate electrode 16. The typical materials of these layers include metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks), which are used with the purpose to improve the electrical characteristics of the device. In a preferred embodiment, a relatively thin layer of titanium nitride (TiN) is deposited on the polysilicon layer 18 to form a barrier layer 20. The barrier layer 20 is then blanketed with a tungsten (W) layer 22 to complete the formation of the gate electrode 16.--

SMC 4/4/07

Please replace the paragraph on page 12, starting at line ⁵2 with the following revised paragraph:

B³

--In forming the source/drain regions 28a and 28b, a first ion implantation is made using the gate electrode 16 and the field isolation regions 12 to mask the substrate, in order to form the more lightly doped portions of LDD source/drain regions 30a and 30b. Generally, although not necessary for the practice of the invention, as shown by FIG. 3c, provided on both sides of the gate electrode 16 are electrode spacers 32. The electrode spacers 32 may be formed from materials including but not limited to insulating materials such as silicon oxides, silicon nitrides and silicon oxynitrides. Various processes are used to form electrode spacers 32. Such processes include Reactive Ion Etch (RIE), and the above mentioned material deposition methods. Typically, electrode spacers 32 are